AMENDMENTS TO THE SPECIFICATION

The paragraph commencing at page 33, line 29 is amended as follows:

As shown in Fig. 10, in a configuration of the semiconductor device of the present embodiment in which first through third seal rings 21 to 23 made up of conductive layers extended in a film-thickness direction of first through fifth wiring insulating films 8, 11, 13, 15, and 16 so as to be electrically connected one after another to the N-type diffusion regions 19 surrounded by an element isolation region 2 are provided as insulated from each other along a periphery of a semiconductor chip 10 in such a manner as to surround a circuit formation portion 18, a second wiring layer 45 and a first via wiring layer 38 that make up a conductive path are formed integrally and simultaneously, while a third wiring layer 59 and a second via wiring layer 52 are formed integrally and simultaneously. It is to be noted that although Fig. ~~9E~~ 10 shows one example of such a configuration that the first seal ring 21 is provided, the second and third seal rings 22 and 23 also have the same configuration.

The paragraph commencing at page 35, line 3 is amended as follows:

The following will describe a method for manufacturing the semiconductor device according to the present embodiment using the dual damascene wiring technology with reference to Figs. 11A and 11B along steps. Note here that the method has been described with reference to one example where only such the first seal ring 21 as shown in Fig. ~~9E~~ 10 is formed.

The paragraph commencing at page 42, line 15 is amended as follows:

It is to be noted that as a specific method for forming the seal ring 71, the single damascene wiring technology employed to form the first through third seal rings 21 to 23 in

the first embodiment described with reference to Figs. ~~9 and 10~~ 9A-9D or the dual damascene wiring technology employed to form the same first through third seal rings 21 to 23 in the second embodiment described with reference to ~~Figs. 12A to 12B~~ Fig. 10 can be applied as it is and so description thereof is omitted.

The paragraph commencing at page 49, line 25 is amended as follows:

According to the semiconductor device of the present embodiment, in a configuration in which a plurality of fuse elements 80 is provided on a surface of a substrate 1 as shown in Figs. 21 and 22, a seal ring 81 made up of conductive layers extended in a film-thickness direction of first through fifth wiring insulating films 8, 11, 13, 15, and 16 so as to be electrically connected to the respective N-type diffusion regions 19 surrounded by an element isolation region 2 is provided endlessly in such a manner as to surround the plurality of the fuse elements 80. The seal ring 81 is formed by connecting a contact 25 electrically connected with the N-type diffusion region 19, a first wiring layer 31, a first via wiring layer 38, a second wiring layer 45, a second via wiring layer 52, and a third wiring layer 59 one after another. The seal ring 81 can be formed specifically by applying a single damascene wiring technology employed to form first through third seal rings 21 to 23 in the first embodiment described with reference to Figs. ~~9 and 10~~ 9A-9D or the dual damascene wiring technology employed to form the same first through third seal rings 21-23 in the second embodiment described with reference to ~~Figs. 11A to 11B~~ Fig. 10.